Abstract of the Disclosure

A multi-phase clock generation circuit includes a clock generation circuit, first frequency divider circuit, first clock selection circuit, second to nth frequency divider circuits, second to nth clock selection circuits, and clock selection control section. The clock generation circuit generates 2^n (n is a positive integer) reference clock signals having the same frequency and different phases. The frequency divider circuit frequency-divides one of the reference clock signals by 2 to generate clock signals 180° out of phase with each other. The first clock selection circuit selects one of each of the clock signals and a corresponding reference clock signal and outputs the selected signals as clock pulses. Each of the second to nth frequency divider circuits frequency-divides a clock pulse to generate clock signals 180° out of phase with each other. Each of the second to nth clock selection circuits selects one of each of the clock signals and a corresponding one of the reference clock signals to output the selected signals as clock pulses. The clock selection control section controls the first to nth clock selection circuits in accordance with a set frequency division ratio.